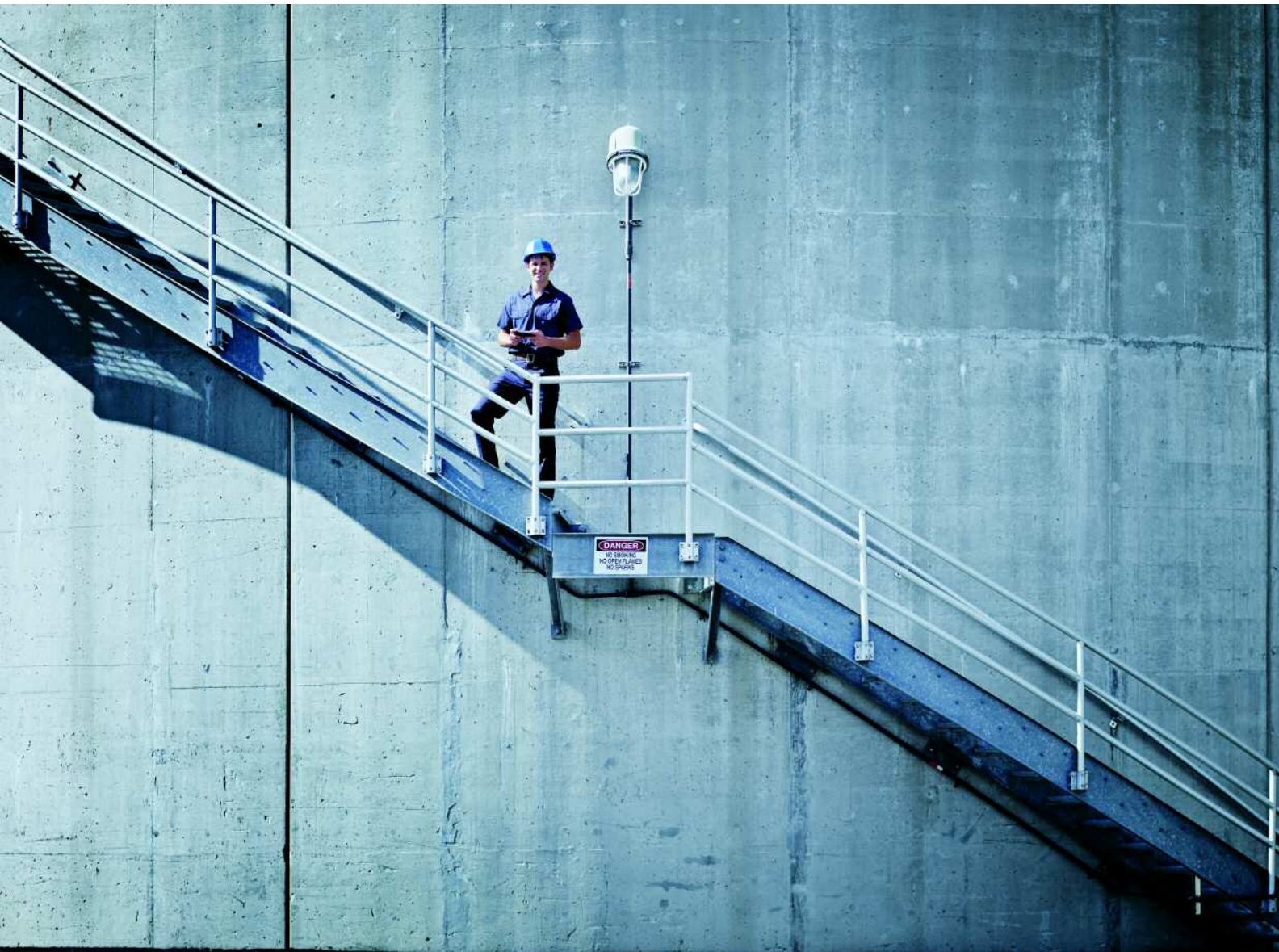
Product Brief
Industrial Control
Reference Design
Embedded Computing

# Intel® Industrial Control Reference Design



## Product Overview

Industrial OEMs, systems integrators and users developing control systems must quickly respond to changing performance, safety and feature requirements, but system architectures based on inflexible 'everything-in-one' ASICs and ASSPs are slowing the pace of redesigns. Whenever there's a need for new functionality or additional performance, a new ASIC or ASSP has to be designed and deployed. Developing these complex chips requires experienced engineers, who are in short supply, and companies can ill-afford to take a trial and error design approach.

Alternatively, functionality can be partitioned into firmware and hardware components, and this architectural approach improves flexibility, scalability and time-to-market. It's relatively easy to reuse or 'mix and match' firmware and hardware components and tailor solutions to specific applications, especially if the architecture is standards-based. There's no long ASIC and ASSP design cycles, and the time required to develop a family of products is greatly reduced.

To meet the need to simplify system development and get to market faster, the Intel® industrial control reference design facilitates the migration to a flexible modular architecture. It's based on an easy-to-use platform, comprising hardware and software components from industrial market leaders.

## The ASIC and ASSP Approach

Although ASIC and ASSP components offer a unique level of integration, it comes at a price. It's possible to put a lot of functionality into a single automation component, as shown in Figure 1, but after the design tapes out, little can be changed. As a result, the component has a high risk of obsolescence because its functionality is fixed and perhaps incapable of satisfying emerging requirements.

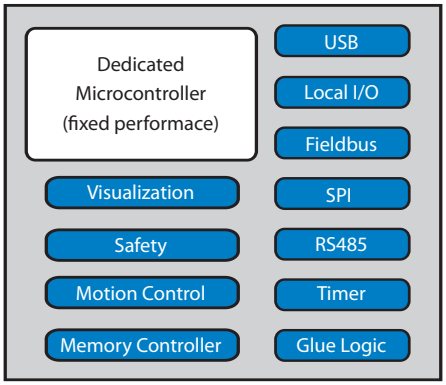



Figure1: ASSP-based Automation Component

Another drawback is that the on-board microcontroller has a fixed level of performance, so users may not be able to add features without jeopardizing real-time response. Furthermore, system developers are locked into one processor architecture for several years, which means they forgo opportunities to benefit from the rapid pace of processor advancement. This ASIC and ASSP approach, with long design cycles and no flexibility to modify existing components, can put system OEMs at a competitive disadvantage.

## A Partitioned Approach

Control systems can be partitioned into commercially-available firmware and hardware components featuring the latest technologies and standards. The example in Figure 2 shows a processor running application software, such as PLC, HMI and motion control, and a fully programmable gate array (FPGA) device implementing various I/O and fieldbus protocols. Since both devices communicate over industry standard PCI Express*, it's straightforward to change out devices and customize the platform for a different set of requirements.

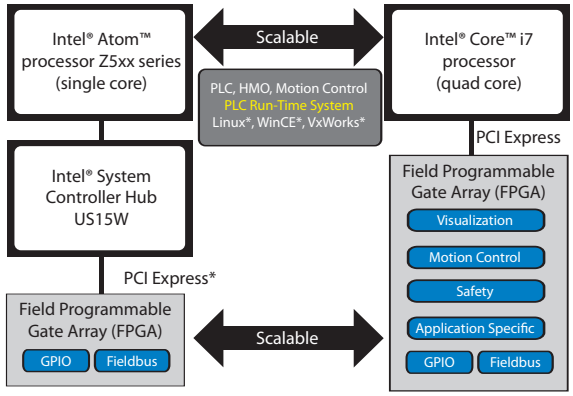



Figure 2: Scalability Example

A new configuration can run legacy firmware with little or no modification, thereby saving development time and cost. This is shown in Figure 2, where software running on the Intel® Atom™ processor (single core) can be easily migrated to the Intel® Core™ i7 processor (4 cores). These processors, combined with FPGAs, yield both low power and high performance platforms and permit a high degree of firmware and hardware reuse. In fact, developers can select from dozens of embedded Intel® Architecture Processors with long-life support and achieve specific cost performance goals.

Intel® processors are backed by the largest development tools and operating system ecosystems in the industry. They also support the highest hardware abstraction level for IEC 61131 systems. For system integrating both control and HMI, Intel® Virtualization Technology (Intel® VT) can securely partition different software applications while maintaining a high level of performance.

## When Flexibility Matters

Who needs the flexibility that system partitioning offers? Consider industrial OEMs, who have to accommodate an abundance of fieldbus solutions used in automation. There are many competing fieldbus technologies, partly due to major suppliers lining up behind different protocols and the particular needs of various application segments: from automotive to industrial control. The lack of a single unified communications approach complicates the development task for OEMs and system integrators, who must master different specs and components.

Since several fieldbus standards have considerable market share, with no significant convergence in sight, suppliers and users are designing, building and maintaining protocol-specific components. There are over twenty-five different real-time Ethernet and fieldbus protocols in use, which strains the supply chain, lengthens design and validation cycles and increases inventory costs. What's needed is a flexible platform that effortlessly supports multiple protocols, thereby reducing the number of line items everyone must manage.

## Industrial Control Reference Design

The joint efforts of Intel, Altera*, MSC* and 3S-Smart Software Solutions* have produced a reference design that delivers real-time performance and I/O flexibility using commercial-off-the-shelf (COTS) components, as shown in Figure 3. Real-time industrial control performance, measured by data latency and bandwidth, is achieved while satisfying aggressive power consumption and form factor requirements. This is accomplished by the Intel Atom processor and its associated chipset , consuming just 4.5 watts TDP total and reducing footprint by more than 80 percent over the previous-generation three-chip solution. The processor system resides on a 70mm x 70mm board supplied by MSC. The board also runs Linux* with real-time extensions that are optimized for machine and plant control systems and are available through the Open Source Automation Development Lab (OSADL: www.osadl.org)

An Altera Arria* GX FPGA interfaces to multiple fieldbus technologies and supports a wide assortment of I/O. The reference design runs the market leading PLC programming IDE from 3S-Smart Software Solutions, called CoDeSys (Controller Development System), based on open international standard IEC 61131. All of these components establish a framework for OEMs and systems integrators to develop their own solutions using COTS building blocks with CAN, CANopen and EtherCAT connectivity (support for Profibus and Profinet to follow).

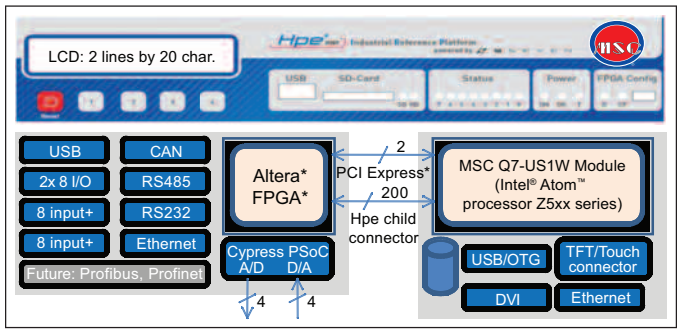



Figure 3. Intel® Industrial Control Reference Design – Block Diagram

## Small and Powerful

The reference design is powered by the MSC Q7-US15W computer-on-module (COM), equipped with the Intel Atom processor and the Intel® System Controller Hub US15W with integrated Intel® Graphics Media Accelerator 500. The module complies with the Qseven* open specification (www.qseven-standard.org). The Q7-US15W, pictured in Figure 4, plugs into an application-specific baseboard and is designed for applications requiring both small form factor and lowest power consumption. There is support for the latest processor and I/O technologies, including PCI Express*, SATA, USB 2.0, LVDS and SVDO interfaces. MSC is a member of the Intel® Embedded and Communications Alliance, and additional information is available at www.msc-ge.com.

Figure 4. The MSC* Q7-US15W Module

## Multiple Busses and Interfaces

The design uses an Altera Arria GX FPGA to implement a large number of interfaces, as shown in Figure 3. This family of FPGAs scales from 180 thousand to three million gates, all fully re-programmable to ensure the highest level of flexibility. Altera offers pre-approved solutions ranging from fieldbus to functional safety, which can decrease OEM development time. In addition, a comprehensive set of tools ensure

developers can implement a successful design quickly and easily through the four S's of success:

**Signal Integrity:** Accelerates high-speed board layout design

**Software Tools:** Increases productivity and shortens design time

**Support Infrastructure:** Helps get designs to market as effortlessly as possible

**Supply:** Based on Stratix II GX transceiver technology and built on TSMC's 90-nm process

The reference design has an Altera USB-Blaster* interface for driving configuration or programming data from the PC to FPGA devices. For more information, please visit www.altera.com.

## PLC Programming

The reference design runs the 3S-Smart Software Solutions' CoDeSys Automation Suite, which is a comprehensive software tool for industrial automation technology. All common automation tasks implemented in software can be realized with the CoDeSys Suite along with companion controller and PLC programming systems. The architecture of CoDeSys can be divided into three basic layers, described below, and additional information is available at www.3s-software.com.

**Development Layer:** The development layer contains the PLC programming system CoDeSys, with the complete online and offline functionality, compilers and components for configuration, visualization and programming.

**Communication Layer:** Communication between the development and the device layer is based on the CoDeSys Gateway Server, which is equipped with an industry standard OPC Server.

**Device Layer:** A runtime system turns any device into a programmable IEC 61131-3 controller and integrated compilers ensure the program code is processed with optimal speed.

## Benefits for Developers

The Intel® Industrial reference design offers significant advantages for developers:

- **Reduced Time-to-Market:** The reference design, supplying basic software, IP and driver foundation, helps reduce development time and simplifies the integration of multiple fieldbus variants.
- **Scalability:** The solution can be migrated to other Intel® architecture platforms, existing and future, with long term availability for all key components.
- **Versatility:** The fanless, cost-effective design, based on well know hardware and software architectures and standard interconnects, can be applied to many different devices.
- **Flexibility:** Modular, programmable I/O components and peripherals ease customization.

**To learn more about Intel® solutions for Industrial Control and Automation, please visit: intel.com/go/industrial**

[1]For the Intel® Core™2 Quad processor, shared L2 cache refers to 6 MB of L2 cache per core pair.



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